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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,166	04/09/2004	Anmol Mathur	CDS-001	2951

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EXAMINER	
LAM, NELSON C	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,166	MATHUR ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *1-4 and 12-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-11 and 16-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication on 04/09/2004. Application 10/822,166 has been examined. In the examination of 10/822,166, claims 5-11 and 16-17 are pending.

Election/Restrictions

2. Applicant's election with traverse of Group II claims 5-11 and 16-17 in the reply filed on 07/05/2006 is acknowledged. The traversal is on the ground(s) that the inventions of Groups I and II are sufficiently related and are classified in the same class with only the subclasses differing. This is not found persuasive because the inventions are independent and require a different field of search.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 5-10 and 16-17 are rejected under 35 U.S.C. 102(e)** as being anticipated by Saluja et al. (US Patent No. 6,772,399).

As per **claim 5**, Saluja discloses a method used in computer-aided circuit design for comparing data flow graphs for equivalence, each data flow graph representing a finite-precision arithmetic circuit (Abstract; col. 2, line 24-36), the data flow graph

comprising a plurality of edges wherein each edge has a finite bit width (Abstract; col. 3, line 58-62), an edge being further connected to a source port and one or more sink ports (col. 3, line 42-49), the source port and the sink ports linked to an edge further connecting the edge to a plurality of arithmetic operators (Abstract; col. 3, line 38-49), each port further having a required precision and an information content associated with it (col. 2, line 24-41), the required precision of a port being the maximum bits of the port observed at any of the output of the port (Fig. 3, #S30; col. 5, line 62-65), the information content of a port being the minimum bits required to represent the output of an arithmetic operation (col. 5, line 62-65), the method comprising the steps of:

a. determining the edges having information loss wherein an edge has an information loss if the information content of the corresponding source port, and the required precision of any of the corresponding sink ports are greater than the bit-width of the edge (Fig. 1A; col. 4, line 16-41);

b. canonizing the data flow graph, the data flow graph being canonized by pushing the arithmetic operations that generate information loss, to the end of the circuit (Fig. 2A-2B; col. 4, line 65 to col. 5, line 17);

c. dividing the data flow graph at edges having information loss, the data flow graphs being split into lossless subgraphs, each lossless subgraph representing an infinite-precision arithmetic circuit (Fig. 2A-2B; col. 4, line 65 to col. 5, line 4);

d. refining the information content of the ports in the data flow graphs, the information content being refined by applying the Huffman Principle and the principles of associativity of addition and multiplication, and the distributivity of multiplication over

addition (Fig. 8, #S335; Fig. 9, #S220; col. 7, line 9-21; col. 9, line 38-46; col. 11, line 11-25; col. 13, line 6-8);

e. verifying the presence of information loss, the information loss being verified at edges corresponding to the ports for which the refinement of information content is performed (Fig. 5, #S125; col. 7, line 45-57);

f. leveling each data flow graph, the level being the order of existence of lossless subgraphs in the data flow graph whereby each data flow graph is leveled for comparison of subgraphs at the same level (Fig. 8, #S326; col. 11, line 9-11);

g. comparing the lossless subgraphs with lowest level number for equality wherein the lossless subgraphs being compared only if the input signal to the data flow graphs have the same bit-width (col. 4, line 65 to col. 5, line 4);

h. comparing the bit-width of the output edges of the lossless subgraphs, the output edges having information loss, wherein the bit-width of the output edges being compared if the preceding lossless subgraphs are compared equal (Fig. 5, #S140, #S145; col. 7, line 58 to col. 8, line 12);

i. comparing the lossless subgraphs with next higher level number for equivalence wherein the comparison of next set of lossless subgraphs being performed if the preceding lossless subgraphs are equal and the bit width of the preceding edges are same (col. 8, line 29-45); and

repeating the steps h and i till the output of the circuit is reached (Fig. 5; col. 8, line 46-50).

As per **claim 6**, Saluja discloses the method as recited in claim 5 further comprises the steps of:

a. computing the required precision of the source port and the sink ports corresponding to each edge wherein the required precision is computed in the reverse topological order of the circuit (Fig. 3, #S30; col. 5, line 62 to col. 6, line 12; Fig. 5, #S145; col. 7, line 58-62); and

b. determining the information content of the source port and the sink ports corresponding to each edge wherein the information content being computed in the topological order of the circuit (Fig. 5, #S145; col. 7, line 58-62).

As per **claim 7**, Saluja discloses the method as recited in claim 6 wherein the step of computing the required precision comprises the steps of:

a. determining the required precision of the sink port of the output signal as the bit width of the signal itself (Fig. 3, #S25; col. 5, line 62-65);

b. determining the required precision at each sink port linked to an arithmetic operator, wherein the required precision is determined as the maximum number of bits observable at the output edge (Fig. 1A; col. 4, line 16-35; Fig. 2A-2B; col. 4, line 65 to col. 5, line 17; col. 6, line 54-64);

c. calculating the minimum of the required precision of the sink port, and the bit width of the corresponding edge for all sets of sink ports of an edge (col. 5, line 18-51); and

d. computing the required precision of the source port as the maximum of the set of minimum values obtained, the minimum values being obtained by comparing the

required precision of the sink port and the bit width of the corresponding edge for all sets of sink ports of an edge (Fig. 3, #S25, #S30; col. 5, line 62 to col. 6, line 12).

As per **claim 8**, Saluja discloses the method as recited in claim 6 wherein the step of determining the information content comprises the steps of:

a. computing the information content at the source port of the input signal as the bit-width of the signal (col. 6, line 54 to col. 7, line 21);

b. calculating the information content of each sink port as the minimum of the information content of the corresponding source port, and the bit width of the corresponding edge (col. 6, line 54 to col. 7, line 21); and

c. computing the information content at a source port linked to an arithmetic operator using the information content at the sink ports linked to the arithmetic operation, as the minimum bit width required to represent the output of the corresponding operator (col. 6, line 54 to col. 7, line 44).

As per **claim 9**, Saluja discloses the method as recited in claim 5 wherein the step of leveling each data flow graph comprises allocating identifiers to lossless subgraphs wherein the identifiers being allocated to lossless subgraphs in topological order (Fig. 8, #S326; col. 11, line 9-11).

As per **claim 10**, Saluja discloses the method as recited in claim 5 wherein the step of comparing the lossless subgraphs for equality comprises the steps of:

a. generating expressions for the data flow graphs (col. 1, line 34-46; col. 9, line 46-65); and

b. checking the equality of expressions, the expressions being checked by theorem proving technique (col. 9, line 36-45).

As per **claim 16**, Saluja discloses a computer program product (Fig. 9; col. 12, line 59-61), the computer program product comprising a computer usable medium having a computer readable program code embodied therein for comparing data flow graphs for equivalence, each data flow graph representing a finite-precision arithmetic circuit (Abstract; col. 2, line 24-36), the data flow graph comprising a plurality of edges wherein each edge has a finite bit width (Abstract; col. 3, line 58-62), an edge being further connected to a source port and one or more sink ports (col. 3, line 42-49), the source port and the sink ports linked to an edge further connecting the edge to a plurality of arithmetic operators (col. 3, line 38-49), each port further having a required precision and an information content associated with it (col. 2, line 24-41) , the required precision of a port being the maximum bits of the port observed at any of the output of the port (Fig. 3, #S30; col. 5, line 62-65), the information content of a port being the minimum bits required to represent the output of an arithmetic operation (col. 5, line 62-65), the computer program code performing steps of:

a. determining the edges having information loss wherein an edge has an information loss if the information content of the corresponding source port, and the required precision any of the corresponding sink ports are greater than the bit-width of the edge (Fig. 1A; col. 4, line 16-41);

b. canonizing the data flow graph, the data flow graph being canonized by pushing the arithmetic operations that generate information loss, to the end of the circuit (Fig. 2A-2B; col. 4, line 65 to col. 5, line 17);

c. dividing the data flow graph at edges having information loss, the data flow graphs being split into lossless subgraphs, each lossless subgraph representing an infinite-precision arithmetic circuit (Fig. 2A-2B; col. 4, line 65 to col. 5, line 4);

d. refining the information content of the ports in the data flow graphs, the information content being refined by applying the Huffman Principle and the principles of associativity of addition and multiplication, and the distributivity of multiplication over addition (Fig. 8, #S335; Fig. 9, #S220; col. 7, line 9-21; col. 9, line 38-46; col. 11, line 11-25; col. 13, line 6-8);

e. verifying the presence of information loss, the information loss being verified at edges corresponding to the ports for which the refinement of information content is performed (Fig. 5, #S125; col. 7, line 45-57);

f. leveling each data flow graph, the level being the order of existence of lossless subgraphs in the data flow graph whereby each data flow graph is leveled for comparison of subgraphs at the same level (Fig. 8, #S326; col. 11, line 9-11);

g. comparing the lossless subgraphs with lowest level number for equality wherein the lossless subgraphs being compared only if the input signal to the data flow graphs have the same bit-width (col. 4, line 65 to col. 5, line 4);

h. comparing the bit-width of the output edges of the lossless subgraphs, the output edges having information loss, wherein the bit-width of the output edges being

compared if the preceding lossless subgraphs are compared equal (Fig. 5, #S140, #S145; col. 7, line 58 to col. 8, line 12); and

i. comparing the lossless subgraphs with next higher level number for equivalence wherein the comparison of next set of lossless subgraphs being performed if the preceding lossless subgraphs are equal and the bit width of the preceding edges are same (col. 8, line 29-45).

As per **claim 17**, Saluja discloses the computer program product described in claim 16, wherein the computer program code further performs the steps of:

a. computing the required precision of the source port and the sink ports corresponding to each edge wherein the required precision is computed in the reverse topological order of the circuit (Fig. 3, #S30; col. 5, line 62 to col. 6, line 12; Fig. 5, #S145; col. 7, line 58-62); and

b. determining the information content of the source port and the sink ports corresponding to each edge wherein the information content being computed in the topological order of the circuit (Fig. 5, #S145; col. 7, line 58-62).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claim 11 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Saluja in view of CVC Lite User Manual. Saluja discloses a method of optimization of

datapaths. However, Saluja does not disclose a CVC program. The CVC Lite User Manual discloses optimization of datapaths using a CVC program that Saluja does not disclose. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a CVC program disclosed in the CVC Lite User Manual in the method of Saluja because a CVC program would aid in the optimization of datapaths (Saluja: col. 1, line 53-59).

As per **claim 11**, Saluja in view of CVC Lite User Manual discloses the method as recited in claim 10 wherein the step of checking the equality of expressions comprises the step of testing the equality using Cooperating Validity Checker Lite (CVC Lite) program (CVC Lite User Manual: Page 1).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday from 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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